AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Dutta et al.	Examiner:	Malzahn, D.
Application No.:	10/005,551	Group Art Unit:	2193
Filed:	November 8, 2001	Docket No.:	US 018181 (VLSI.331PA)
Title:	High-Speed Computation in Arithmetic Logic Circuit		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on June 28, 2006.

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REPLY BRIEF

Board of Patent Appeals and Interferences
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Sir:

This is a Reply Brief submitted pursuant to 37 C.F.R. § 41.41(a)(1) for the above-referenced patent application. Appellant requests that the appeal of the instant application be maintained. If necessary, authority is given to charge/credit Deposit Account No. 50-0996 (VLSI.331PA) 50-0996 any fees/overages in support of this filing.

The content of this Reply Brief complies with the requirements set forth in MPEP § 1208(I), specifically the modified requirements A-D.

I. Status of Claims

Claims 1-20 are pending, of which claims 1-19 stand rejected and claim 20 has been allowed.

II. Grounds of Rejection to be Reviewed

A. The rejection of claims 1-19 should be reversed because the '157 reference does not correspond to the claimed limitations directed to a multiplexer.

B. The rejection of claims 1-19 should be reversed because the '157 reference does not correspond to the claimed limitations directed to selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

C. The rejection of claim 4 should be reversed because the new assertion of inherency (presented in the Examiner's Answer) is unsupported by any reference and fails to provide correspondence to the claimed limitations.

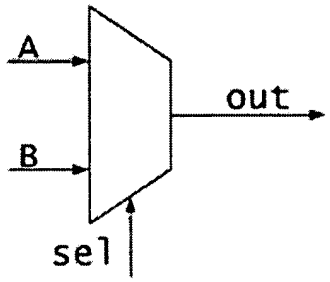
D. The rejections of dependent claims 2-17 should be reversed because the Examiner failed to mention various claimed limitations, much less reference any portion of the '157 reference that corresponds to these limitations.

III. Argument

A. The rejection of claims 1-19 should be reversed because the '157 reference does not correspond to claimed limitations directed to a multiplexer or multiplexer functions.

In the Office Actions of record, the Examiner failed to identify where the '157 reference teaches basic claim limitations including those directed to a multiplexer that provides the claimed output in response to selection data, by passing the claimed inputs. The Examiner's Answer specifically asserts that the '157 reference's selective enablement of one of two components to a common location, namely an increment/decrement network (INCH) and temporary register (TEMPH) to a bus (ABH), corresponds to (*i.e.*, is) a multiplexer. This suggestion is untenable. As discussed in prior Office Actions of record, the '157 reference simply does not describe, show or otherwise correspond to a multiplexer. Moreover, from a functional perspective, the '157 reference separately controls the enablement of each of the referenced INCH 12 and TEMPH 16 (*see* FIGs. 1 and 7), making a multiplexer inapplicable to its operation. That is, there is no selection or control of the output of any signal at a multiplexer or other selection circuit because each of INCH 12 and TEMPH 16 is coupled directly to the bus ABH 10. Instead of selecting between available output signals, the '157 reference separately controls the enablement of the INCH 12 or the TEMPH 16.

In digital circuit design, a multiplexer is a device that has multiple input streams and only one output stream. It forwards one of the input streams to the output stream based on the values of one or more "selection inputs." *See, e.g.*, www.wikipedia.com. An example visual representation of these multiple inputs and single output to a multiplexer device is shown below.



In the above representation, "sel" is selection data which is an input along with the "A" and "B" streams.

Referring particularly to FIGs. 1 and 7 of the '157 reference and the multiplexer figure above, the cited portions of the '157 reference clearly do not correspond to a multiplexer. In the multiplexer figure above, signals "A" and "B" are passed to the multiplexer. The multiplexer then passes one of signals "A" and "B" as an output in accordance with a selection signal. Contrary to the above example, signals from each of the INCH 12 and TEMPH 16 in the '157 reference never pass to a multiplexer. Instead, the ALU 28 selectively enables each of the INCH 12 and TEMPH 16 to the ACH 10 using separate enable signals 126 and 127 (*see, e.g.*, FIG. 7 and column 11, lines 43-46). The ALU 28 controls this enablement of one of the INCH 12 or TEMPH 16 onto the bus ABH 10 via data bus DB 6. *See, e.g.*, column 3, line 63 through column 4, line 6; column 4, lines 47-63 and FIG. 1. In this regard, signal selection is controlled at the source of the signal, rather than at a downstream location, and there is no selection made for passing one of two received signals at a common location (multiplexer). In short, signals from the INCH 12 and TEMPH 16 are simply not passed to a multiplexer or any selection circuit that, in turn, selectively passes one of the two signals to the bus ABH 10.

In view of the above, the rejections of claims 1-19 should be reversed because the cited '157 reference does not disclose a multiplexer or multiplexer functions.

B. The rejection of claims 1-19 should be reversed because the '157 reference does not correspond to the claimed limitations directed to selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

The above discussion with Ground A should be dispositive of the claim rejections, as the cited portions of the '157 do not correspond to a multiplexer or multiplexer functionality. However, the rejections of claims 1-19 are also improper because the Examiner failed to identify the use of any selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand in a manner consistent with any claim rejections. For example, in attempting to arrive at the claimed limitations, the Examiner references the last line of the Abstract as support for the assertion that "selection

data for the multiplexer is a function of the most-significant bit of the set of least-significant bits ...." However, this assertion is misplaced because the "most significant" language in the referenced portion of the Abstract is directed to a "most significant byte" that is provided as a result of a selection, not as data used to make a selection. That is, according to the '157 Abstract, the alleged selection data is a function of the carry signal and the sign bit of the second binary operand. Therefore, this cited portion of the '157 reference appears to have no relevance to any selection data as claimed.

In addition to the above, when applying the '157 teachings to claim 1, for example, the first binary operand has N bits and the second operand has M bits, where N must be equal to or greater than M. Therefore, the first operand of the '157 reference is 16 bits and the second operand is 8 bits. Thus, the referenced "sign bit of the 8-bit operand" fails to correspond to the claimed selection data because it is a function of the second binary operand (the 8-bit operand).

In view of the above, the rejections of claims 1-19 should also be reversed because the cited '157 reference does not correspond to limitations directed to selection data as claimed, for a multiplexer or otherwise.

C. The rejection of claim 4 should be reversed because the new assertion of inherency (presented in the Examiner's Answer) is unsupported by any reference and fails to provide correspondence to the claimed limitations.

As discussed in the Appeal Brief, the Examiner fails to assert or identify any correspondence between any of the dependent claims and the '157 reference, and specifically with limitations in claim 4 directed to the first binary operand (N) being 24 bits and the second binary operand (M) being 16 bits. The Examiner's Answer acknowledges that the '157 reference does not call for these limitations, but goes on to suggest that the limitations are "inherent in Daniel because Daniel speaks in terms of bytes, i.e. 8 bits, and his example is N being 16 and M being 8." This discussion fails to show or even allege any correspondence between the '157 and the claimed limitations, is unsupported by any prior art reference and is unsupported in the '157 reference itself. Therefore, the rejection of claim 4 is improper and should be removed.

D. The rejections of dependent claims 2-17 should be reversed because the Examiner failed to mention various claimed limitations, much less reference any portion of the '157 reference that corresponds to these limitations.

The Examiner failed to address the dependent claim limitations in any of the Office Actions of record. In this regard, the Examiner also failed to cite any portion of the '157 reference (or any reference) that corresponds to these dependent claim limitations. The Examiner's Answer first addresses certain limitations, in claim 4 as discussed with Ground 3 above, and for claims 11, 15 and 16. However, various other claimed limitations remain unaddressed. This (late) discussion of limitations in the Examiner's Answer, and failure to address Appellant's traversals as well as the limitations in other dependent claims is contrary to 35 U.S.C. §132 and the M.P.E.P., in that the Appellant has not been afforded the opportunity to address the rejections. Moreover, the assertions in the Examiner's Answer regarding claims 15 and 16 fail to cite any portion of the '156 reference and, instead, are broad conclusions unsupported by any evidence (*e.g.*, that Daniels system "can operate on unsigned binary numbers" and that "a digital filtering circuit arrangement" is merely intended use). Therefore, the dependent claim rejections should also be reversed for these reasons.

VIII. Conclusion

Appellant maintains that the claimed invention is patentable over the cited references, and that the claim rejections must be reversed. Appellant respectfully requests from the Board of Patent Appeals that the above issues be addressed and incorporated into the rendering of your Decision.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Should there be any issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

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